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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
SHEW, JOHN	

ART UNIT	PAPER NUMBER
2616	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/032,729	CHEN ET AL.	
	Examiner	Art Unit	
	John L. Shew	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-46 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,11-39 and 41-45* is/are rejected.

7)☒ Claim(s) *10,40 and 46* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *3/9/2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to because

FIG. 4, referenced character "420" is used to identify two different processing steps. The specification discusses the same identifier for two different processing steps (page 14 para. [0037], page 15 para. [0038]-[0039]). One of the duplicated identifiers should be renumbered and the specification corrected accordingly.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application

must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 3, 31, 32, 33, 41, 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Basso et al. (Pub. No. US 2002/0154634 A1) in view of Tezuka (Patent No. US 6658014 B1).

Claim 1, Basso teaches a method comprising storing packet data within a storage element (Fig. 5, page 5 para. [0084]-[0085]) referenced by Buffers 505_1 – 505_5 to store packet data, maintaining a transmit count value of said storage element (Fig. 5, page 5 para. [0084]-[0085]) referenced by MultiCast Counter to determine when all instances have been transmitted, comparing said transmit count value and a release count value

(Fig. 5, page 5 para. [0084]-[0085]) referenced by the comparison of the MCC to the value of zero, and de-allocating said storage element in response to comparing said transmit count value and a release count value (Fig. 5, page 5 para. [0084]-[0086]) referenced by the discard of Frame Control Block 501 and its associated buffers 505_1 – 505_5 by returning them to the free FCB and free buffer queues. Basso does not teach determining a release count value of said storage element.

Tezuka teaches determining a release count value of storage elements (Fig. 19A, col. 16 lines 17-31, Fig. 23, col. 18 lines 60-67, col. 19 lines 15) referenced by the Release Count Designation Unit 22-4 in comparison to a Threshold Value Designation Unit 22-3 for identifying the number of discrete storage buffers for output.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the packet buffer device of Tezuka to the Multicast Data Structure of Basso for the purpose of providing a method for optimally assigning the buffer capacity of a common buffer type and a discrete buffer type to achieve optimal use of buffer resources as suggested by Tezuka (col. 3 lines 12-15).

Claim 2, Basso teaches receiving a packet including said packet data (Fig. 2, page 3 para. [0059], page 4 para. [0060]) referenced by the reception of data packets from the Ethernet MAC interface 203 to the Dataflow chip 202, and allocating said storage element in response to receiving said packet (Fig. 2, page 3 para. [0059], page 4 para. [0060], [0069]) referenced by the Dataflow chip 202 interfacing to a large Datastore Memory 205 for buffering of traffic.

Claim 3, Basso teaches transmitting said packet data from said storage element (Fig. 2, page 4 para. [0069]) referenced by the large Datastore Memory 205 as repository for frames awaiting retransmission and multiple DRAM interfaces to provide sustained transmit and receive bandwidth for the port interface.

Claim 31, arguments analogous to those stated in the rejection of claim 1 are applicable.

Basso teaches a machine-readable medium (Fig. 3, page 4 para. [0060]-[0062]) referenced by the PowerPC microprocessor core 304 to interface with a SRAM instruction store , which when executed by a set of one or more processors (page 4 para. [0061]) referenced by the twelve Dyadic Protocol Processor Units, to perform operations comprising storing packet data within a storage element (Fig. 5, page 5 para. [0084]-[0085]) referenced by Buffers $505_1 - 505_5$ to store packet data.

Claim 32, arguments analogous to those stated in the rejection of claim 2 are applicable.

Claim 33, arguments analogous to those stated in the rejection of claim 3 are applicable.

Claim 41, Basso teaches a method comprising storing a plurality of packet data within a plurality of storage elements (Fig. 5, page 5 para. [0084]-[0085]) referenced by Buffers $505_1 - 505_5$ to store a plurality of packet data, maintaining a transmit count value of each one of said plurality of storage elements (Fig. 5, page 5 para. [0084]-[0085]) referenced by MultiCast Counter MCC for each packet to determine when all instances have been transmitted from the respective buffers, comparing said transmit count value and a release count value (Fig. 5, page 5 para. [0084]-[0085]) referenced by the comparison of the MCC to the value of zero, and de-allocating each one of said plurality of storage elements in response to comparing said transmit count value and a release count value (Fig. 5, page 5 para. [0084]-[0086]) referenced by the discard of Frame Control Block 501 and its associated buffers $505_1 - 505_5$ by returning them to the free FCB and free buffer queues. Basso does not teach determining a release count value of said storage element. does not teach determining a release count value of each one of said plurality of storage elements.

Tezuka teaches determining a release count value of of each one of said plurality of storage elements (Fig. 10, col. 11 lines 14-25, Fig. 19A, col. 16 lines 17-31, Fig. 23, col. 18 lines 60-67, col. 19 lines 15) referenced by the Release Count Designation Unit 22-4 in comparison to a Threshold Value Designation Unit 22-3 for identifying the number of discrete storage buffers for output wherein there are a plurality of discrete storage buffers for different buffer types.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the packet buffer device of Tezuka to the Multicast Data

Structure of Basso for the purpose of providing a method for optimally assigning the buffer capacity of a common buffer type and a discrete buffer type to achieve optimal use of buffer resources as suggested by Tezuka (col. 3 lines 12-15).

Claim 42, Basso teaches further comprising transmitting each one of said plurality of packet data from said plurality of storage elements (Fig. 2, page 4 para. [0069], Fig. 5, page 5 para. [0084]-[0086]) referenced by the large Datastore Memory 205 as repository for frames awaiting retransmission and multiple DRAM interfaces to provide sustained transmit and receive bandwidth for the port interface wherein the Reference Frame Control Block has a Multicast Counter MCC for each plurality of packet data respectively.

Claims 4, 5, 6, 7, 9, 11, 12, 13, 14, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 30, 34, 35, 36, 37, 39, 43, 44, 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Basso and Tezuka as applied to claims 1, 3 above, and further in view of Gulick (Patent No. 4809269).

Claim 4, Basso teaches wherein maintaing a transmit count value of said storage element (Fig. 5, page 5 para. [0084]-[0085]) referenced by MultiCast Counter to

determine when all instances have been transmitted, comprises initializing said transmit count value (Fig. 5, page 5 para. [0084]-[0085, page 6 para. [0104]-[0106]) referenced by MultiCast Counter value stored by the Dataflow Chip based on the multicast action. Basso does not teach incrementing said transmit count value by one in response to transmitting said packet data.

Gulick teaches incrementing said transmit count value by one in response to transmitting said packet data (Fig. 5, col. 10 lines 29-58) referenced by the Transmit Byte Counter 154 receiving a COUNT signal upon a Transmit FIFO buffer 150 output and comparison of the Transmit Byte Counter 154 to a Threshold Comparison Logic 158 to determine if the end count threshold is reached.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the Dual Port Timing Controller of Gulick to the Packet Buffer Multicast Data Structure of Basso and Tezuka for the purpose of providing control signals allowing ordinary RAM to be operated as an S-RAM as suggested by Gulick (col. 1 lines 57-60).

Claim 5, Basso teaches wherein comparing said transmit count value and a release count value (Fig. 5, page 5 para. [0084]-[0085]) referenced by the comparison of the MCC to the value of zero, comprises de-allocating said storage element in response to comparing said transmit count value and a release count value (Fig. 5, page 5 para. [0084]-[0086]) referenced by the discard of Frame Control Block 501 and its associated buffers $505_1 - 505_5$ by returning them to the free FCB and free buffer queues. does not

teach the determining whether an incremented transmit count value is equal to a release count value.

Gulick teaches determining whether an incremented transmit count value is equal to a release count value (Fig. 5, col. 10 lines 29-58) referenced by the Transmit Byte Counter 154 is compared to the Threshold Comparison Logic 158 to determine if the threshold count is reached.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the Dual Port Timing Controller of Gulick to the Packet Buffer Multicast Data Structure of Basso and Tezuka for the purpose of providing control signals allowing ordinary RAM to be operated as an S-RAM as suggested by Gulick (col. 1 lines 57-60).

Claim 6, Basso teaches wherein transmitting said packet data from said storage element (Fig. 2, page 4 para. [0069]) referenced by the large Datastore Memory 205 as repository for frames awaiting retransmission and multiple DRAM interfaces to provide sustained transmit and receive bandwidth for the port interface, comprises transmitting said packet data from said storage element via a plurality of output interfaces (Fig. 2, Fig. 5, page 5 para. [0084]-[0086]) referenced by the multicast transmission of three instances to three destinations wherein the output queues may be queued for transmission via different ports.

(col. 1 lines 57-60).

repository for frames awaiting retransmission and multiple DRAM interfaces to provide

Claim 7, Basso teaches wherein transmitting said packet data from said storage element (Fig. 2, page 4 para. [0068]-[0069]) referenced by the large Datastore Memory 205 as repository for frames awaiting retransmission and multiple DRAM interfaces to provide sustained transmit and receive bandwidth for the port interface, via a plurality of output interfaces (Fig. 2, Fig. 5, page 5 para. [0084]-[0086]) referenced by the multicast transmission of three instances to three destinations wherein the output queues may be queued for transmission via different ports, comprises transmitting said packet data from said storage element via a plurality of line interfaces (Fig. 2, page 4 para. [0068]-[0069]) referenced by the interconnections between the Data Store 205 and the Dataflow chip 202 and ultimate transfer to the Ethernet MAC 203.

Claim 9, Basso teaches said packet data including a packet header (Fig. 4, page 5 para. [0075]-[0083]) referenced by the Message ID and Message Parameters, and a packet body (Fig. 4, page 5 para. [0075]-[0083]) referenced by the Data, wherein storing packet data within a storage element (Fig. 5, page 5 para. [0084]-[0085]) referenced by Buffers 505_1 – 505_5 to store packet data, comprises storing said packet body within a common storage element (Fig. 5, page 5 para. [0084]-[0085]) referenced by Buffers 505_1 – 505_5 to store packet data, storing a copy of said packet header within a unique storage element for each of said plurality of output interfaces (Fig. 5, page 6 para. [0090]) referenced by the unique data for the instance written to the Frame Alteration Control Block 503 for different header data to different output ports, and associating

each of said plurality of unique storage elements with said common storage element (Fig. 5) referenced by the linkage of the FACB 503 to the Buffers $505_1 - 505_5$.

Claim 11, Basso teaches an apparatus comprising an input module to store packet data within a storage element (Fig. 2, page 3 para. [0059], page 4 para. [0060], [0069]) referenced by the reception of data packets from the input Ethernet MAC interface 203 to the Dataflow chip 202 which interfaces to a large Datastore Memory 205 for buffering of traffic, and to initialize a transmit count value of said storage element (Fig. 5, page 5 para. [0084]-[0085], page 6 para. [0104]-[0106]) referenced by MultiCast Counter value stored by the Dataflow Chip based on the multicast action, a direct memory access controller to transmit said packet data from said storage element (Fig. 2, page 3 para. [0059], page 4 para. [0060], [0069]) referenced by the Dataflow chip 202 which transfer data between the Datastore Memory 205 and the Ethernet MAC interface 203, and to de-allocate said storage element in response to a determination that said transmit count value is equal to a release count value (Fig. 5, page 5 para. [0084]-[0086]) referenced by the comparison of the MCC to the value of zero followed by the discard of Frame Control Block 501 and its associated buffers $505_1 - 505_5$ by returning them to the free FCB and free buffer queues. Basso does not teach a processing element to determine a release count value of said storage element.

Tezuka teaches a processing element to determine a release count value of storage elements (Fig. 19A, col. 16 lines 17-31, Fig. 23, col. 18 lines 60-67, col. 19 lines 15) referenced by the Release Count Designation Unit 22-4 in comparison to a Threshold

value is equal to a release count value (Fig. 5, page 5 para. [0084]-[0086]) referenced

Value Designation Unit 22-3 for identifying the number of discrete storage buffers for output.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the packet buffer device of Tezuka to the Multicast Data Structure of Basso for the purpose of providing a method for optimally assigning the buffer capacity of a common buffer type and a discrete buffer type to achieve optimal use of buffer resources as suggested by Tezuka (col. 3 lines 12-15).

Basso and Tezuka do not teach a memory controller to increment said transmit count value by one in response to a transmission of said packet data.

Gulick teaches a memory controller incrementing said transmit count value by one in response to transmitting said packet data (Fig. 5, col. 10 lines 29-58) referenced by the Transmit Byte Counter 154 receiving a COUNT signal upon a Transmit FIFO buffer 150 output and comparison of the Transmit Byte Counter 154 to a Threshold Comparison Logic 158 to determine if the end count threshold is reached.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the Dual Port Timing Controller of Gulick to the Packet Buffer Multicast Data Structure of Basso and Tezuka for the purpose of providing control signals allowing ordinary RAM to be operated as an S-RAM as suggested by Gulick (col. 1 lines 57-60).

Claim 12, Basso teaches wherein said input module to store packet data within a storage element (Fig. 2, page 3 para. [0059], page 4 para. [0060], [0069]) referenced by

the reception of data packets from the input Ethernet MAC interface 203 to the Dataflow chip 202 which interfaces to a large Datastore Memory 205 for buffering of traffic, and to initialize a transmit count value of said storage element (Fig. 5, page 5 para. [0084]-[0085, page 6 para. [0104]-[0106]) referenced by MultiCast Counter value stored by the Dataflow Chip based on the multicast action, comprises an input module to receive a packet (Fig. 2, page 3 para. [0059]) referenced by the Ethernet MAC interface 203, including said packet data (Fig. 4) referenced by the message Data, and to allocate said storage element for said packet including said packet data (Fig. 2, page 3 para. [0059], page 4 para. [0060], [0069]) referenced by the Dataflow chip 202 interfacing to a large Datastore Memory 205 for buffering of traffic.

Claim 13, Basso teaches wherein said direct memory access controller to transmit said packet data from said storage element (Fig. 2, page 3 para. [0059], page 4 para. [0060], [0069]) referenced by the Dataflow chip 202 which transfer data between the Datastore Memory 205 and the Ethernet MAC interface 203, comprises a direct memory access controller to transmit said packet data from said storage element via a plurality of output interfaces (Fig. 2, Fig. 5, page 5 para. [0084]-[0086]) referenced by the multicast transmission of three instances to three destinations wherein the output queues may be queued for transmission via different ports.

Claim 14, Basso teaches wherein said direct memory access controller to transmit said packet data from said storage element (Fig. 2, page 3 para. [0059], page 4 para.

[0060], [0069]) referenced by the Dataflow chip 202 which transfer data between the Datastore Memory 205 and the Ethernet MAC interface 203, via a plurality of output interfaces (Fig. 2, Fig. 5, page 5 para. [0084]-[0086]) referenced by the multicast transmission of three instances to three destinations wherein the output queues may be queued for transmission via different ports, comprises a direct memory access controller to transmit said packet data from said storage element via a plurality of line interfaces (Fig. 2, page 3 para. [0059]) referenced by the Ethernet MAC interface 203 of various transmission protocol rates.

Claim 16, Basso teaches said packet data including a packet header (Fig. 4, page 5 para. [0075]-[0083]) referenced by the Message ID and Message Parameters, and a packet body (Fig. 4, page 5 para. [0075]-[0083]) referenced by the Data, wherein said input module to store packet data within a storage element (Fig. 2, page 3 para. [0059], page 4 para. [0060], [0069]) referenced by the reception of data packets from the input Ethernet MAC interface 203 to the Dataflow chip 202 which interfaces to a large Datastore Memory 205 for buffering of traffic, and to initialize a transmit count value of said storage element (Fig. 5, page 5 para. [0084]-[0085, page 6 para. [0104]-[0106]) referenced by MultiCast Counter value stored by the Dataflow Chip based on the multicast action, comprises an input module to store said packet body within a common storage element (Fig. 5, page 5 para. [0084]-[0085]) referenced by Buffers 505_1 – 505_5 to store packet data, comprises a processing element to store a copy of said packet header within a unique storage element for each of said plurality of output interfaces

(Fig. 5, page 6 para. [0090]) referenced by the unique data for the instance written to the Frame Alteration Control Block 503 for different header data to different output ports, and to associate each of said plurality of unique storage elements with said common storage element (Fig. 5) referenced by the linkage of the FACB 503 to the Buffers $505_1 - 505_5$. Basso does not teach said processing element to determine a release count value of said storage element.

Tezuka teaches a processing element to determine a release count value of storage elements (Fig. 19A, col. 16 lines 17-31, Fig. 23, col. 18 lines 60-67, col. 19 lines 15) referenced by the Release Count Designation Unit 22-4 in comparison to a Threshold Value Designation Unit 22-3 for identifying the number of discrete storage buffers for output.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the packet buffer device of Tezuka to the Multicast Data Structure of Basso for the purpose of providing a method for optimally assigning the buffer capacity of a common buffer type and a discrete buffer type to achieve optimal use of buffer resources as suggested by Tezuka (col. 3 lines 12-15).

Claim 17, Basso teaches an apparatus comprising a first line card to transmit data to a communications network (Fig. 2, page 3 para. [0059]) referenced by the Ethernet MAC interface 203, a line card interconnect coupled to said first line card and a second line card coupled to said line card interconnect (Fig. 2, page 3 para. [0059]) referenced by the interconnection between the Ethernet MAC interface 203 and the Dataflow Chip

202, to receive data from a communications network (Fig. 2, page 3 para. [0059], page 4 para. [0060]) referenced by the Dataflow Chip 202 transmitting and receiving traffic via network port, said second line card including an input module to store packet data within a storage element (FIG. 2, page 3 para. [0059], page 4 para. [0060]) referenced by the Embedded Processor Complex 209 to control the data storage through lookup tables and processing of headers, and to initialize a transmit count value of said storage element (Fig. 5, page 5 para. [0084]-[0085], page 6 para. [0106]) referenced by the MultiCast Counter whose value is assigned by the Dataflow Chip 202, a direct memory access controller to transmit said packet data from said storage element (Fig. 2, page 3 para. [0059], page 4 para. [0060], [0069]) referenced by the Dataflow chip 202 which transfer data between the Datastore Memory 205 and the Ethernet MAC interface 203, and to de-allocate said storage element in response to a determination that said transmit count value is equal to a release count value (Fig. 5, page 5 para. [0084]-[0086]) referenced by the comparison of the MCC to the value of zero followed by the discard of Frame Control Block 501 and its associated buffers $505_1 - 505_5$ by returning them to the free FCB and free buffer queues. Basso does not teach a memory controller to increment said transmit count value by one in response to a transmission of said packet data. does not teach a processing element to determine a release count value of said storage element.

Tezuka teaches a processing element to determine a release count value of storage elements (Fig. 19A, col. 16 lines 17-31, Fig. 23, col. 18 lines 60-67, col. 19 lines 15) referenced by the Release Count Designation Unit 22-4 in comparison to a Threshold

Value Designation Unit 22-3 for identifying the number of discrete storage buffers for output.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the packet buffer device of Tezuka to the Multicast Data Structure of Basso for the purpose of providing a method for optimally assigning the buffer capacity of a common buffer type and a discrete buffer type to achieve optimal use of buffer resources as suggested by Tezuka (col. 3 lines 12-15).

Basso and Tezuka do not teach a memory controller to increment said transmit count value by one in response to a transmission of said packet data.

Gulick teaches a memory controller incrementing said transmit count value by one in response to transmitting said packet data (Fig. 5, col. 10 lines 29-58) referenced by the Transmit Byte Counter 154 receiving a COUNT signal upon a Transmit FIFO buffer 150 output and comparison of the Transmit Byte Counter 154 to a Threshold Comparison Logic 158 to determine if the end count threshold is reached.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the Dual Port Timing Controller of Gulick to the Packet Buffer Multicast Data Structure of Basso and Tezuka for the purpose of providing control signals allowing ordinary RAM to be operated as an S-RAM as suggested by Gulick (col. 1 lines 57-60).

Claim 18, Basso teaches said second line card (Fig. 2, page 3 para. [0059]) referenced by the Dataflow Chip 202, further including a line interface module to receive data from

a communications network (Fig. 2, page 3 para. [0059]) referenced by the Dataflow chip 202 interface to the Ethernet MAC interface 203, wherein said input module to store packet data within a storage element (FIG. 2, page 3 para. [0059], page 4 para. [0060]) referenced by the Embedded Processor Complex 209 to control the data storage through lookup tables and processing of headers, and to initialize a transmit count value of said storage element (Fig. 5, page 5 para. [0084]-[0085], page 6 para. [0106]) referenced by the MultiCast Counter whose value is assigned by the Dataflow Chip 202, comprises an input module to receive a packet including said packet data from said line interface module (Fig. 2, page 3 para. [0059], page 4 para. [0060]-[0061]) referenced by the Embedded Processor Complex 209 receiving packet data from the Ethernet MAC interface 203 for table lookup with the Dataflow chip 202 storing the packet in the Datastore Memory 205, and to allocate said storage element for said packet including said packet data (Fig. 5, page 5 para. [0084]-[0085]) referenced by Buffers $505_1 - 505_5$ allocated to store packet data.

Claim 19, Basso teaches said second line card (Fig. 2, page 3 para. [0059]) referenced by the Dataflow Chip 202, further including a memory coupled to said memory controller to store said storage element (Fig. 2, page 3 para. [0059], page 4 para. [0060], [0069]) referenced by the Dataflow chip 202 which acts as a memory controller to transfer data between the Datastore Memory 205 and the Ethernet MAC interface 203.

Claim 20, Basso teaches said second line card (Fig. 2, page 3 para. [0059]) referenced by the Dataflow Chip 202, further including a line card interconnect interface module having a plurality of output interfaces coupled to said line card interconnect (Fig. 2, page 3 para. [0059]) referenced by the Dataflow Chip 202 interconnection with the Ethernet MAC interface 203 which carries a plurality of output ports including 1xOC-192c 4xOC-48c 16xOC-12c 1x10Gb Ethernet and 10x1Gb Ethernet.

Claim 21, Basso teaches wherein said direct memory access controller to transmit said packet data from said storage element (Fig. 2, page 3 para. [0059], page 4 para. [0060], [0069]) referenced by the Dataflow chip 202 which transfer data between the Datastore Memory 205 and the Ethernet MAC interface 203, comprises a direct memory access controller to transmit said packet data from said storage element to said line card interconnect interface module (Fig. 2, page 3 para. [0059], page 4 para. [0060], [0069]) referenced by the Dataflow chip 202 which transfer data between the Datastore Memory 205 and the Ethernet MAC interface 203 through the interconnection between the Dataflow chip 202 and the Ethernet MAC interface 203.

Claim 22, Basso teaches wherein said direct memory access controller to transmit said packet data from said storage element (Fig. 2, page 3 para. [0059], page 4 para. [0060], [0069]) referenced by the Dataflow chip 202 which transfer data between the Datastore Memory 205 and the Ethernet MAC interface 203, comprises a direct memory access controller to transmit said packet data from said storage element via a plurality

of output interfaces (Fig. 2, Fig. 5, page 5 para. [0084]-[0086]) referenced by the multicast transmission of three instances to three destinations wherein the output queues may be queued for transmission via different ports.

Claim 23, Basso teaches said packet data including a packet header (Fig. 4, page 5 para. [0075]-[0083]) referenced by the Message ID and Message Parameters, and a packet body (Fig. 4, page 5 para. [0075]-[0083]) referenced by the Data, wherein said input module to store packet data within a storage element (Fig. 2, page 3 para. [0059], page 4 para. [0060], [0069]) referenced by the reception of data packets from the input Ethernet MAC interface 203 to the Dataflow chip 202 which interfaces to a large Datastore Memory 205 for buffering of traffic, and to initialize a transmit count value of said storage element (Fig. 5, page 5 para. [0084]-[0085, page 6 para. [0104]-[0106]) referenced by MultiCast Counter value stored by the Dataflow Chip based on the multicast action, comprises an input module to store said packet body within a common storage element (Fig. 5, page 5 para. [0084]-[0085]) referenced by Buffers $505_1 - 505_5$ to store packet data, comprises a processing element to store a copy of said packet header within a unique storage element for each of said plurality of output interfaces (Fig. 5, page 6 para. [0090]) referenced by the unique data for the instance written to the Frame Alteration Control Block 503 for different header data to different output ports, and to associate each of said plurality of unique storage elements with said common storage element (Fig. 5) referenced by the linkage of the FACB 503 to the [illegible] storage element (Fig. 5, page 5 para. [illegible] page 6 para. [illegible] Chip [illegible]

Buffers $505_1 - 505_5$. Basso does not teach said processing element to determine a release count value of said storage.

Tezuka teaches a processing element to determine a release count value of storage elements (Fig. 19A, col. 16 lines 17-31, Fig. 23, col. 18 lines 60-67, col. 19 lines 15) referenced by the Release Count Designation Unit 22-4 in comparison to a Threshold Value Designation Unit 22-3 for identifying the number of discrete storage buffers for output.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the packet buffer device of Tezuka to the Multicast Data Structure of Basso for the purpose of providing a method for optimally assigning the buffer capacity of a common buffer type and a discrete buffer type to achieve optimal use of buffer resources as suggested by Tezuka (col. 3 lines 12-15).

Claim 24, arguments analogous to those stated in the rejection of claim 17 are applicable.

Claim 25, arguments analogous to those stated in the rejection of claim 18 are applicable.

Claim 26, arguments analogous to those stated in the rejection of claim 19 are applicable.

Claim 27, arguments analogous to those stated in the rejection of claim 20 are applicable.

Claim 28, Basso teaches wherein said direct memory access controller to transmit said packet data from said storage element (Fig. 2, page 3 para. [0059], page 4 para. [0060], [0069]) referenced by the Dataflow chip 202 which transfer data between the Datastore Memory 205 and the Ethernet MAC interface 203, comprises a direct memory access controller to transmit said packet data from said storage element via said plurality of output interfaces (Fig. 2, page 3 para. [0059], page 4 para. [0060], [0069]) referenced by the Dataflow chip 202 which transfer data between the Datastore Memory 205 and the Ethernet MAC interface 203 which has a plurality of output ports including 1xOC-192c 4xOC-48c 16xOC-12c 1x10Gb Ethernet and 10x1Gb Ethernet.

Claim 30, arguments analogous to those stated in the rejection of claim 23 are applicable.

Claim 34, arguments analogous to those stated in the rejection of claim 4 are applicable.

Claim 35, arguments analogous to those stated in the rejection of claim 5 are applicable.

Claim 36, arguments analogous to those stated in the rejection of claim 6 are applicable.

Claim 37, arguments analogous to those stated in the rejection of claim 7 are applicable.

Claim 39, arguments analogous to those stated in the rejection of claim 9 are applicable.

Claim 43, Basso teaches wherein maintaining a transmit count value of said plurality of storage elements (Fig. 5, page 5 para. [0084]-[0085]) referenced by MultiCast Counter to determine when all instances have been transmitted for each FCB, comprises initializing said transmit count value (Fig. 5, page 5 para. [0084]-[0085, page 6 para. [0104]-[0106]) referenced by MultiCast Counter value stored by the Dataflow Chip based on the multicast action. Basso and Tezuka do not teach incrementing said transmit count value by one in response to transmitting said packet data. Gulick teaches incrementing said transmit count value by one in response to transmitting said packet data (Fig. 5, col. 10 lines 29-58) referenced by the Transmit Byte Counter 154 receiving a COUNT signal upon a Transmit FIFO buffer 150 output and comparison of the Transmit Byte Counter 154 to a Threshold Comparison Logic 158 to determine if the end count threshold is reached.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the Dual Port Timing Controller of Gulick to the Packet Buffer Multicast Data Structure of Basso and Tezuka for the purpose of providing control signals allowing ordinary RAM to be operated as an S-RAM as suggested by Gulick (col. 1 lines 57-60).

Claim 44, Basso teaches wherein transmitting each one of said plurality of packet data from said plurality of storage elements (Fig. 2, page 4 para. [0069]) referenced by the large Datastore Memory 205 as repository for multicast frames awaiting retransmission and multiple DRAM interfaces to provide sustained transmit and receive bandwidth for the port interface, comprises transmitting each one of said plurality of packet data from one of said plurality of storage elements via a plurality of output interfaces (Fig. 2, Fig. 5, page 5 para. [0084]-[0086]) referenced by the multicast transmission of three instances to three destinations wherein the output queues may be queued for transmission via different ports.

Claim 45, Basso teaches each one of said plurality of packet data including a packet header (Fig. 4, page 5 para. [0075]-[0083]) referenced by the Message ID and Message Parameters, and a packet body (Fig. 4, page 5 para. [0075]-[0083]) referenced by the Data, wherein storing said plurality of packet data within a storage element (Fig. 5, page 5 para. [0084]-[0085]) referenced by Buffers 505_1 – 505_5 to store packet data, comprises storing said packet body within a common storage element (Fig. 5, page 5

para. [0084]-[0085]) referenced by Buffers $505_1 - 505_5$ to store packet data, storing a copy of said packet header within a unique storage element for each of said plurality of output interfaces (Fig. 5, page 6 para. [0090]) referenced by the unique data for the instance written to the Frame Alteration Control Block 503 for different header data to different output ports, and associating each of said plurality of unique storage elements with said common storage element (Fig. 5) referenced by the linkage of the FACB 503 to the Buffers $505_1 - 505_5$.

3. Claims 8, 15, 29, 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Basso, Tezuka and Gulick as applied to claims 1, 3, 4, 6, 7, 11, 13, 14, 24, 27, 28 above, and further in view of Chow et al. (Patent No. US 6269081 B1).

Claim 8, Basso teaches wherein transmitting said packet data from said storage element (Fig. 2, page 4 para. [0068]-[0069]) referenced by the large Datastore Memory 205 as repository for frames awaiting retransmission and multiple DRAM interfaces to provide sustained transmit and receive bandwidth for the port interface, via a plurality of line interfaces (Fig. 2, page 4 para. [0068]-[0069], Fig. 5, page 5 para. [0084]-[0086]) referenced by the multicast transmission of three instances to three destinations wherein the output queues may be queued for transmission via different ports and by the interconnections between the Data Store 205 and the Dataflow chip 202 with

ultimate transfer to the Ethernet MAC 203, comprises transmitting said packet data from said storage element via a line interface (Fig. 2, page 4 para. [0068]-[0069]) referenced by the interconnections between the Data Store 205 and the Dataflow chip 202 and ultimate transfer to the Ethernet MAC 203, selected from the group consisting of an Ethernet interface (Fig. 2, page 3 para. [0059]) referenced by the Ethernet MAC interface 203, a Fast Ethernet Interface (Fig. 2, page 3 para. [0059]) referenced by the Ethernet MAC interface 203 with 10Gb Ethernet, a Gigabit Ethernet interface (Fig. 2, page 3 para. [0059]) referenced by the Ethernet MAC interface 203 with 10x1Gb Ethernet, an OC-48/STM-16 interface (Fig. 2, page 3 para. [0059]) referenced by the Packet Over Sonet interface 203 with 4xOC-48c, an OC-12/STM-14 interface (Fig. 2, page 3 para. [0059]) referenced by the Packet Over Sonet interface 203 with 16xOC-12c, an OC-3/STM-1. Basso, Tezuka and Gulick do not teach an OC-3/STM-1 interface, an IF Video interface, a DS-1 interface, a DS-3 interface, an E-1 interface and an E-3 interface.

Chow teaches an OC-3/STM-1 interface (Fig. 1, col. 6 lines 7-45) referenced by the OC-3 of 1.6 Gbps Access Shelf 3B, an IF Video interface (Fig. 1, col. 6 lines 7-45) referenced by the FastBus Video of 800Mbps Access Shelf 3C, a DS-1 interface (Fig. 1, col. 6 lines 7-45) referenced by DS-1 of 800Mbps Access Shelf 3D, a DS-3 interface (Fig. 1, col. 6 lines 7-45) referenced by the DS-3 of 800Mbps Access Shelf 3C, an E-1 interface (Fig. 1, col. 6 lines 7-45) referenced by the E-1 of 800Mbps Access Shelf 3D, and an E-3 interface (Fig. 1, col. 6 lines 7-45) referenced by the E-3 of 800Mbps Access Shelf 3C.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the Switching Core interfaces of Chow to the Multicast Data Structure of Basso, Tezuka and Gulick for the purpose of maximizing utilization of a switching core by providing a variable number of universal card slots depending on the interface card bandwidth as suggested by Chow (col. 4 lines 50-54).

Claim 15, Basso teaches wherein said direct memory access controller to transmit said packet data from said storage element (Fig. 2, page 3 para. [0059], page 4 para. [0060], [0069]) referenced by the Dataflow chip 202 which transfer data between the Datastore Memory 205 and the Ethernet MAC interface 203, via a plurality of line interfaces (Fig. 2, page 3 para. [0059]) referenced by the Ethernet MAC interface 203 of various transmission protocol rates, comprises a direct memory access controller to transmit said packet data from said storage element via a line interface (Fig. 2, page 4 para. [0068]-[0069]) referenced by the interconnections between the Data Store 205 and the Dataflow chip 202 and ultimate transfer to the Ethernet MAC 203, selected from the group consisting of an Ethernet interface (Fig. 2, page 3 para. [0059]) referenced by the Ethernet MAC interface 203, a Fast Ethernet Interface (Fig. 2, page 3 para. [0059]) referenced by the Ethernet MAC interface 203 with 10Gb Ethernet, a Gigabit Ethernet interface (Fig. 2, page 3 para. [0059]) referenced by the Ethernet MAC interface 203 with 10x1Gb Ethernet, an OC-48/STM-16 interface (Fig. 2, page 3 para. [0059]) referenced by the Packet Over Sonet interface 203 with 4xOC-48c, an OC-12/STM-14 interface (Fig. 2, page 3 para. [0059]) referenced by the Packet Over Sonet interface

203 with 16xOC-12c. Basso, Tezuka and Gulick do not teach an OC-3/STM-1 interface, an IF Video interface, a DS-1 interface, a DS-3 interface, an E-1 interface and an E-3 interface.

Chow teaches an OC-3/STM-1 interface (Fig. 1, col. 6 lines 7-45) referenced by the OC-3 of 1.6 Gbps Access Shelf 3B, an IF Video interface (Fig. 1, col. 6 lines 7-45) referenced by the FastBus Video of 800Mbps Access Shelf 3C, a DS-1 interface (Fig. 1, col. 6 lines 7-45) referenced by DS-1 of 800Mbps Access Shelf 3D, a DS-3 interface (Fig. 1, col. 6 lines 7-45) referenced by the DS-3 of 800Mbps Access Shelf 3C, an E-1 interface (Fig. 1, col. 6 lines 7-45) referenced by the E-1 of 800Mbps Access Shelf 3D, and an E-3 interface (Fig. 1, col. 6 lines 7-45) referenced by the E-3 of 800Mbps Access Shelf 3C.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the Switching Core interfaces of Chow to the Multicast Data Structure of Basso, Tezuka and Gulick for the purpose of maximizing utilization of a switching core by providing a variable number of universal card slots depending on the interface card bandwidth as suggested by Chow (col. 4 lines 50-54).

Claim 29, Basso teaches wherein said direct memory access controller to transmit said packet data from said storage element (Fig. 2, page 3 para. [0059], page 4 para. [0060], [0069]) referenced by the Dataflow chip 202 which transfer data between the Datastore Memory 205 and the Ethernet MAC interface 203, via a plurality of output (Fig. 2, page 3 para. [0059]) referenced by the Ethernet MAC interface 203 of various

ports carrying different transmission protocol rates, comprises a direct memory access controller to transmit said packet data from said storage element via a line interface (Fig. 2, page 4 para. [0068]-[0069]) referenced by the interconnections between the Data Store 205 and the Dataflow chip 202 and ultimate transfer to the Ethernet MAC 203, selected from the group consisting of an Ethernet interface (Fig. 2, page 3 para. [0059]) referenced by the Ethernet MAC interface 203, a Fast Ethernet Interface (Fig. 2, page 3 para. [0059]) referenced by the Ethernet MAC interface 203 with 10Gb Ethernet, a Gigabit Ethernet interface (Fig. 2, page 3 para. [0059]) referenced by the Ethernet MAC interface 203 with 10x1Gb Ethernet, an OC-48/STM-16 interface (Fig. 2, page 3 para. [0059]) referenced by the Packet Over Sonet interface 203 with 4xOC-48c, an OC-12/STM-14 interface (Fig. 2, page 3 para. [0059]) referenced by the Packet Over Sonet interface 203 with 16xOC-12c. Basso, Tezuka and Gulick do not teach an OC-3/STM-1 interface, an IF Video interface, a DS-1 interface, a DS-3 interface, an E-1 interface and an E-3 interface.

Chow teaches an OC-3/STM-1 interface (Fig. 1, col. 6 lines 7-45) referenced by the OC-3 of 1.6 Gbps Access Shelf 3B, an IF Video interface (Fig. 1, col. 6 lines 7-45) referenced by the FastBus Video of 800Mbps Access Shelf 3C, a DS-1 interface (Fig. 1, col. 6 lines 7-45) referenced by DS-1 of 800Mbps Access Shelf 3D, a DS-3 interface (Fig. 1, col. 6 lines 7-45) referenced by the DS-3 of 800Mbps Access Shelf 3C, an E-1 interface (Fig. 1, col. 6 lines 7-45) referenced by the E-1 of 800Mbps Access Shelf 3D, and an E-3 interface (Fig. 1, col. 6 lines 7-45) referenced by the E-3 of 800Mbps Access Shelf 3C.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the Switching Core interfaces of Chow to the Multicast Data Structure of Basso, Tezuka and Gulick for the purpose of maximizing utilization of a switching core by providing a variable number of universal card slots depending on the interface card bandwidth as suggested by Chow (col. 4 lines 50-54).

Claim 38, arguments analogous to those stated in the rejection of claim 8 are applicable.

Allowable Subject Matter

Claims 10, 40, 46 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

The applicant's arguments traversing the rejections of claims 1 and 31 has been fully considered. Basso does not disclose the limitation "determining a release count". The examiner respectfully maintains the Basso teachings on the remaining limitations. A new prior art search reveals Tezuka discloses a processing element which "determines a release count". Comparision with the release count as a separate count value is performed, thus there are two separate counters. Claims 1, 31 are rejected under 35 USC § 103 as being obvious by Basso in view of Tezuka.

The applicant's arguments to claims 2-10, 32-40, 11, 17, 24, 12-16, 18, 23, 25-30, 41-46 are analogous to the arguments pertaining to claims 1,31 in that Basso does not teach two separate counters. Hence the response is the same as for claims 1, 31 above.

Regarding the new claims 41-46 and the limitation of a "plurality of packet data within a plurality of storage elements", Basso teaches this limitation (Fig. 5) in so far that each Reference Frame Control Block carries a MCC value. There is more than a single FCB for the system and each FCB carries a MCC for the packet string, thus the plurality of packet data within a plurality of storage elements.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John L. Shew whose telephone number is 571-272-3137. The examiner can normally be reached on 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema Rao can be reached on 571-272-3174. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Seema S. Rao 5/11/06

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